Amendments to the Drawings:

The attached sheet of drawing includes a change to Figure 5. This sheet replaces the original Figure 5.

Attachments: Replacement Sheet

REMARKS

Applicant respectfully requests reconsideration of the Application as amended. Claims 1-28 are pending. Applicants have amended claims 7, 11, 14, 21, 25 and 28. No claims have been added. No new matter has been added.

Specification

The Office Action states that the title of the invention is not descriptive and suggested a new title. The specification has been amended to adopt the suggested title.

Drawings

The Office Action objected to the drawings because they included reference characters not mentioned in the description. Accordingly, Applicant has remove element 510 from Figure 5 and added to the description reference to elements 74 and 84 in Figure 7B (please see Specification Amendment). Applicant respectfully requests that the Examiner withdraw the objection.

Claim Objections

The Office Action has objected to claims 7-14 and 21-28 because of informalities. Applicant has amended the claims to correct the informalities. Applicant respectfully requests that the Examiner withdraw the objection.

Claim Rejections – 35 USC § 102(e)

The Office Action rejected claims 1-20 as being anticipated by Popescu et al U.S. patent 5,625,837 (herein referred to as Popescu).

The present invention as claimed in claims 1, 7 and 15 requires among other limitations "decoding a test instruction with a second instance of said first destination register where said second instance of said fist destination register is decoded as a first source register" and "validating results of said advanced load instruction using said test

instruction with said first physical register." (Emphasis added). Applicant respectfully submits that Popescu does not teach, mention, nor disclose such a limitation.

Specifically, Popescu describes a processor architecture "which operates with improved computational efficiency using instruction fetching functions that are decoupled from instruction execution functions by a dynamic register file." (Abstract, Popescu).

The Office Action states that Popescu describes the limitations described above at column 10, lines 58-61. There, Popescu describes a way to make sure that the most up-to-date values are read from register file 17 to source registers RX and RY of an instruction. This is done by searching the destination (RZ of instructions) register addresses of younger instructions in the dynamic register file to make sure that an update to register file 17 is not pending at the addresses named by RX and RY. (Popescu at column 10, lines 58-68). In other words, Popescu's description describes searching for conflicts between sources and destinations of different instructions in order to avoid loading erroneous data. At this section, Popescu does not mention, "decoding a test instruction", where a "second instance of said fist destination register is decoded as a first source register." (Emphasis added). Applicant cannot find any other location in Popescu that teaches such a limitation.

The Office Action states that Popescu describes, at column 11, lines 1-3, the use of a "valid bit" in a result register of the dynamic register The "valid bit" of Popescu is described in the context of determining whether an instruction can read the value of a destination register of an instruction from the dynamic register file 11 instead of having to load it from the register file 17. (Popescu at column 11 lines 1-6). The "valid bit" is set to invalid when "one or both of its operands have not been generated by older instructions." (Popescu, column 11, lines 1-18).

Furthermore, unlike Popescu, the present invention as claimed requires "validating results of said advanced load instruction using said test instruction with said first physical register." (emphasis added). Thus, the use of the "valid bit" in Popescu is not the same as the claim limitations.

Accordingly, Applicants respectfully submit that Popescu does not set forth the present invention as claimed in claims 1, 7 and 15 require and thus the present invention as claimed is not anticipated.

Claims 2-6, 8-14, and 16-20 are dependent upon claims 1, 7, and 15 respectively and therefore are allowable for at least the same reasons.

Claim Rejections – 35 USC § 103

The Office Action rejected claims 21-28 as being unpatentable over Popescu in view of Witt (U.S. Patent 6,189,068 B1) (herein referred to as Witt). Applicant respectfully disagrees.

Witt describes a "superscalar microprocessor employing a data cache configured to perform store accesses in a single clock cycle." (Witt, Abstract). Witt also describes a processor coupled to a sound card. (Witt, column 193, lines 15-17).

As set forth above, Popescu at least does not describe a "decoder to decode a test instruction with a first instance of a first destination register corresponding to an advanced load instruction with a second instance of said first destination register wherein said first instance is decoded as a first source register" Witt does not overcome this deficiency. Thus, the Office Action does not set forth a combination that decodes a test instruction with first instance of a first destination register as first source register.

Accordingly, Applicants respectfully submit that the present invention as claimed is not obvious in view of the combination of Popescu and Witt. Claims 21-28 are dependent upon claims 20 and are allowable for at least the same reason.

CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance, for which early action is earnestly solicited.

Invitation for a telephone interview

The Examiner is invited to call the undersigned at 408-720-8300 if there remains any issue with allowance of this case.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 7/6, 2006

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